REMARKS

The Applicants request reconsideration of the rejection. Claims 15-20, 28-29, and 32-37 are now pending.

Claims 15-37 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,731,167. The Applicants traverse as follows.

The present invention relates to a high frequency power amplifier module which has a high frequency power amplifier having first and second amplifying systems including a plurality of amplifying states (Q1, Q2 and Q4, Q5), a bias control circuit (BIAS CONTROL CIRCUIT), a first input terminal (Pin-GSM), a second input terminal (Pin-DCS), a first output terminal (Pout-GSM), and a second output terminal (Pout-DCS). See, for example, the specification at page 6, lines 1-15, and Fig. 19.

The first amplifying system, second amplifying system, and bias control circuit are monolithically formed on a single semiconductor chip (FET CHIP) which is mounted on a module. See Figs. 19-21. This provides advantages of reduced surface area and improved power efficiency, in addition to the advantages provided by the high frequency power amplifier

module itself. See, for example, page 35, lines 1-5 of the specification.

Claims 1-14 of the subject patent, however, do not require the bias control circuit to be formed monolithicall on a single semiconductor chip with the high frequency power amplifying systems. Thus, in light of the advantages brought by the invention as now claimed, it is believed that no double patenting rejection is warranted.

Claims 15-17, 21-31, and 34 were rejected under 35 U.S.C. §102(e) as being anticipated by Tsutsui, et al., US 6,636,114 (Tsutsui). The Applicants traverse as follows.

Tsutsui discloses a high frequency power amplifier module ahving input and output terminals, control terminals, a mode switch terminal, mode switching elements, and a high frequency power amplifier having first and second amplifying sytems and a bias circuit. See Fig. 6.

The first amplifying stystem includes a plurality of amplifying stages cascade-connected between an input terminal Pin-GSM900 and an output terminal Pout-GSM900, and the second amplifying system includes a plurality of amplifying stages casecade-connected between an input terminal Pin-GSM1800 and an output terminal Pout-GSM1800. A bias circuit including resistance leements R3, R7, R10 and R16, R20, R23 and a

plurality of termperature characteristic compensating circuites Tr 4, 5, 6 and Tr 16, 17, 18 are provided for the respective amplifying stages.

However, Tsutsui fails to disclose the relationship in which the first and second amplifying stages and the bias circuit are monolithically formed on a single semiconductor chip, which is required to meet the newly-amended claims. Further, Tsutsui describes a dual-gate FET or FET connected in series in a source-drain path as the first amplifying stage, whereas claim 15 requires each amplifying stage to include a MOSFET of a first conductivity type and a gate coupled to the corresponding first bias terminal. Accordingly, the Applicants submit that the claims are not met by Tsutsui.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,

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